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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/782,997	02/19/2004	John A. Smythe III	MICRON.278A	7124

20995 7590 01/12/2006

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EXAMINER	
NOVACEK, CHRISTY L	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/782,997	SMYTHE ET AL.	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-56* is/are pending in the application.

4a) Of the above claim(s) *48-56* is/are withdrawn from consideration.

5)☒ Claim(s) *27-34* is/are allowed.

6)☒ Claim(s) *1-26,35-41,46 and 47* is/are rejected.

7)☒ Claim(s) *42-45* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/10/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the Election filed October 25, 2005.

Election/Restrictions

Applicant's election of claims 1-47 in the paper filed October 25, 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claims 48-56 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the paper filed October 25, 2005.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 6, 8-14, 16-22, 25, 26, 35-41, 46 and 47 are rejected under 35 U.S.C. 102(e) as being anticipated by Ahn et al. (US 6,699,799).

Regarding claim 1, Ahn discloses etching a trench in a substrate (10), wherein the trench has a base and walls, depositing an amorphous silicon liner (49) on surfaces of the trench, filling

the trench with a dielectric material (51), and densifying the dielectric material with a process that will cause the liner to become oxidized (col. 5, ln. 51 – col. 6, ln. 16). Ahn does not specifically disclose that oxidation of the amorphous silicon liner causes the liner to expand. However, Applicant's specification states that amorphous silicon expands uniformly upon oxidation (para. 0021). Therefore, it appears that oxidation of the amorphous silicon liner of Ahn will inherently cause the liner to expand.

Regarding claim 6, Ahn discloses depositing a nitride layer (47) on the substrate before depositing the liner and after etching the trench (col. 5, ln. 60-61).

Regarding claim 8, Ahn discloses depositing an insulating oxygen barrier layer (47) on the substrate before depositing the liner and after etching the trench (col. 5, ln. 60-61).

Regarding claims 9 and 10, Ahn discloses that the liner is made of amorphous silicon and the liner is oxidized. Ahn does not specifically disclose that oxidation of the amorphous silicon liner causes the liner to expand. However, Applicant's specification states that amorphous silicon expands uniformly upon oxidation (para. 0021). Therefore, it appears that oxidation of the amorphous silicon liner of Ahn will inherently cause the liner to expand.

Regarding claims 11 and 12, Ahn discloses that the amorphous silicon liner is 50-300 Å thick (col. 5, ln. 64-66).

Regarding claims 13, Ahn discloses that filling dielectric material in the trench is done by applying a liquid to the substrate (col. 4, ln. 20-46).

Regarding claim 14, Ahn discloses that filling dielectric material in the trench is done by using a spin-on deposition process (col. 5, ln. 66 – col. 6, ln. 6).

Regarding claims 16, 17, 46 and 47, Ahn discloses that densifying the dielectric material causes shrinkage of approximately 20% (col. 5, ln. 2-4).

Regarding claim 18, Ahn discloses that densifying the dielectric material involves oxidizing the dielectric material (col. 5, ln. 7-9).

Regarding claim 19, Ahn discloses oxidizing the liner, which inherently expands the liner (col. 6, ln. 10-15).

Regarding claim 20, Ahn discloses that the oxidizing includes curing in a steam ambient environment in a curing chamber (col. 2, ln. 49-61).

Regarding claim 21, Ahn discloses that the curing can begin at an initial temperature of 80-350°C (col. 4, ln. 49-50).

Regarding claim 22, Ahn discloses that the curing can be completed at a target temperature of 700-1000°C (col. 4, ln. 56-57).

Regarding claims 25 and 26, Ahn discloses annealing the substrate in an oxygen environment for 10-60 minutes at a temperature of 1000°C.

Regarding claim 35, Ahn discloses lining a trench with an amorphous silicon liner (49), filling the trench with a dielectric filler (51), and densifying the dielectric material with a process that will cause the liner to become oxidized (col. 5, ln. 51 – col. 6, ln. 16). Ahn does not specifically disclose that oxidation of the amorphous silicon liner causes the liner to expand. However, Applicant's specification states that amorphous silicon expands uniformly upon oxidation (para. 0021). Therefore, it appears that oxidation of the amorphous silicon liner of Ahn will inherently cause the liner to expand.

Regarding claim 36, Ahn discloses lining the trench with an oxygen barrier (47) before lining the trench with an expandable liner.

Regarding claim 37, Ahn discloses that the oxygen barrier layer is made of silicon nitride.

Regarding claim 38, Ahn discloses that the expandable liner is made of amorphous silicon.

Regarding claim 39, Ahn discloses that the dielectric filler is applied as a liquid.

Regarding claim 40, Ahn discloses that the dielectric filler is applied by spin-on deposition.

Regarding claim 41, Ahn discloses that expanding the liner while contracting the filler involves oxidation.

Claims 35, 38 and 41 are rejected under 35 U.S.C. 102(b) as being anticipated by Yu et al. (US 5,869,384).

Regarding claim 35, Yu discloses lining a trench with an expandable liner, filling the trench with a dielectric filler, and expanding the liner while contracting the filler (Abstract; col. 6, ln. 56 – col. 8, ln. 25).

Regarding claim 38, Yu discloses that the expandable liner can be amorphous silicon (col. 7, ln. 9-11).

Regarding claim 41, Yu discloses that expanding the liner while contracting the filler is done by oxidation (col. 8, ln. 7-13).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (US 6,699,799) in view of Kim et al. (US 6,461,937).

Regarding claim 2, Ahn discloses forming an oxide layer (41) on the surface of the substrate before etching the trench, but Ahn does not disclose how the oxide layer is formed. Like Ahn, Kim discloses a process of forming a shallow trench isolation structure in a semiconductor substrate. Kim teaches that a pad oxide can be formed on the substrate by thermally oxidizing the surface of the substrate (col. 5, ln. 49-52). At the time of the invention, it would have been obvious to one of ordinary skill in the art to thermally oxidize the substrate of Ahn to form the pad oxide layer, as is taught by Kim, because Ahn does not teach any particular method of forming the pad oxide and formation of the pad oxide by thermal oxidation is well-known and conventional in the art.

Regarding claim 3, Ahn discloses depositing a layer of silicon nitride (43) over the pad oxide before etching the trench.

Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (US 6,699,799) in view of Hokozono (US 6,956,276).

Regarding claim 4, Ahn discloses etching the trench but does not disclose the etching method. Like Ahn, Hokozono discloses a process of forming a shallow trench isolation structure

in a semiconductor substrate. Hokozono teaches that the trench can be formed in the substrate by etching the substrate using RIE (col. 9, ln. 45-52). At the time of the invention, it would have been obvious to one of ordinary skill in the art to etch the substrate of Ahn to form a trench using RIE because Ahn does not teach any particular method of etching the trench and Hokozono teaches the RIE can successfully etch the shallow isolation trench.

Regarding claim 5, Ahn discloses oxidizing the walls of the trench to form an oxide layer (45).

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (US 6,699,799) in view of Lee et al. (US 6,500,726).

Regarding claim 7, Ahn does not disclose the thickness of the nitride layer. Like Ahn, Lee discloses forming a shallow trench isolation structure having a nitride oxidation barrier layer therein. Lee discloses that in order to serve as a successful oxidation barrier layer, the nitride layer should have a thickness of 50-100Å thick (col. 6, ln. 58-66). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the nitride layer of Ahn such that it is 50-100Å thick because Ahn discloses using the nitride layer as an oxidation barrier layer and Lee discloses that a nitride layer used as an oxidation barrier layer should have a thickness of 50-100Å.

Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (US 6,699,799).

Regarding claims 23 and 24, Ahn does not disclose the rate at which the temperature is changed from its initial curing temperature to its final cure temperature. At the time of the

invention, it would have been obvious to one of ordinary skill in the art to use routine experimentation to determine an appropriate temperature ramping rate for the curing step disclosed by Ahn, depending upon the cure time and the amount of solvent in the SOG layer.

Claims 1-5, 9-12 and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (US 5,869,384) in view of Hokozono (US 6,956,276).

Regarding claim 1, Yu discloses forming a trench in a substrate (10), wherein the trench has a base and walls, depositing a liner (16) on surfaces of the trench, filling the trench with a dielectric material (18), and densifying the dielectric material with a process that will cause the liner to expand (Abstract; col. 6, ln. 56 – col. 8, ln. 25). Yu does not specifically disclose etching the substrate to form the trench. Like Yu, Hokozono discloses a process of forming a shallow trench isolation structure in a semiconductor substrate. Hokozono teaches that the trench can be formed in the substrate by etching the substrate (col. 9, ln. 45-52). At the time of the invention, it would have been obvious to one of ordinary skill in the art to etch the substrate of Yu to form a trench, as is taught by Hokozono, because Yu does not teach any particular method of forming the trench and formation of the trench by etching is well-known and conventional in the art.

Regarding claims 2 and 3, Yu discloses growing a layer of thermal oxide (12a/12b/12c) on the surface of the wafer and depositing a layer of silicon nitride (14a/14b/14c) over the thermal oxide, but Yu does not specifically disclose that these layers are formed before etching the trench (col. 6, ln. 13-16). Hokozono teaches a shallow trench isolation is formed by depositing an oxide layer on the surface of the substrate, depositing a nitride layer on the oxide layer and then using lithography to etch the trench. At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the thermal oxide and nitride layers of Yu

on the substrate before etching the trench, as is taught by Hokozono, in order that the nitride layer can be used as a mask for etching the trench.

Regarding claim 4, Hokozono discloses that the trench is etched using RIE (col. 9, ln. 45-49).

Regarding claim 5, Yu discloses that the inside of the trench is oxidized after trench formation (col. 6, ln. 29-35).

Regarding claim 9, Yu discloses that the liner expands upon oxidation (col. 8, ln. 7-13).

Regarding claim 10, Yu discloses that the liner can be amorphous silicon (col. 7, ln. 9-11).

Regarding claim 11, Yu discloses that the amorphous silicon liner is about 150-250 Å thick (col. 7, ln. 9-11).

Regarding claim 12, Yu does not disclose that the thickness of the amorphous silicon liner is 50-100 Å. Yu discloses that the amorphous silicon liner is oxidized to compensate for the densification of the oxide trench fill material. Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use routine experimentation to determine an appropriate thickness for the amorphous silicon liner layer, depending upon how much the trench fill material densifies.

Regarding claim 15, Yu discloses that the trench fill dielectric material is deposited using a chemical vapor deposition process (col. 7, ln. 21-34).

Regarding claims 16 and 17, Yu discloses densifying the dielectric material, but does not disclose the exact amount of densification. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use routine experimentation to determine an

appropriate amount of densification of the dielectric material, depending upon the length and temperature of the densification anneal.

Regarding claim 18, Yu discloses that the dielectric material is densified in an oxygen atmosphere, and, thereby, the liner is oxidized. But Yu does not specifically disclose that the dielectric material is oxidized. However, because the dielectric material is subjected to an anneal in an oxygen atmosphere, it appears that the dielectric material will inherently be oxidized to some degree.

Regarding claim 19, Yu discloses that expanding the liner is performed by oxidizing the liner (col. 8, ln. 7-8).

Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (US 5,869,384) in view of Hokozono (US 6,956,276), as applied to claim 1 above, and further in view of Lee et al. (US 6,500,726).

Regarding claims 6 and 8, Yu does not disclose depositing a nitride layer on the substrate before depositing the liner and after etching the trench. Like Yu, Lee discloses a process of forming a shallow trench isolation structure in a semiconductor substrate. Lee teaches that it is conventional in the art to form an insulating nitride layer over the inside of the trench prior to deposition of the isolation fill layer because the nitride layer serves the purpose of acting as an oxygen barrier, thereby preventing the sides of the trench from oxidizing and damaging the substrate (col. 1, ln. 20-40). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form a nitride layer in the trench of Yu before forming the liner, as is taught by Lee, because Lee teaches that the nitride layer offers the advantage of preventing the substrate from oxidizing.

Regarding claim 7, Lee discloses that the nitride layer is preferably 50-100Å thick (col. 6, ln. 58-66).

Claims 36 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (US 5,869,384) in view of Lee et al. (US 6,500,726).

Regarding claims 36 and 37, Yu does not disclose depositing a nitride layer on the substrate before depositing the liner and after etching the trench. Like Yu, Lee discloses a process of forming a shallow trench isolation structure in a semiconductor substrate. Lee teaches that it is conventional in the art to form an insulating silicon nitride layer over the inside of the trench prior to deposition of the isolation fill layer because the nitride layer serves the purpose of acting as an oxygen barrier, thereby preventing the sides of the trench from oxidizing and damaging the substrate (col. 1, ln. 20-40). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form a silicon nitride layer in the trench of Yu before forming the liner, as is taught by Lee, because Lee teaches that the nitride layer offers the advantage of preventing the substrate from oxidizing.

Claims 46 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (US 5,869,384).

Regarding claims 46 and 47, Yu discloses densifying the dielectric material, but does not disclose the exact amount of densification. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use routine experimentation to determine an appropriate amount of densification of the dielectric material, depending upon the length and temperature of the densification anneal.

Allowable Subject Matter

Claims 27-34 are allowed.

Claims 42-45 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The primary reason for the allowance of claims 27-34 and the indication of the allowable subject matter of claims 42-45 is the inclusion therein, in combination as currently claimed, of the limitation of curing the dielectric material in a steam ambient at a temperature of 200-600°C and ramping up to 800-1200°C. This limitation is found in claims 27-34 and 42-45 and is neither disclosed nor taught by the prior art of record, alone or in combination.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
January 6, 2006

ZANDRA V. SMITH
SUPERVISORY PATENT EXAMINER